3A Ultra Low Dropout Linear Regulator

❖ GENERAL DESCRIPTION

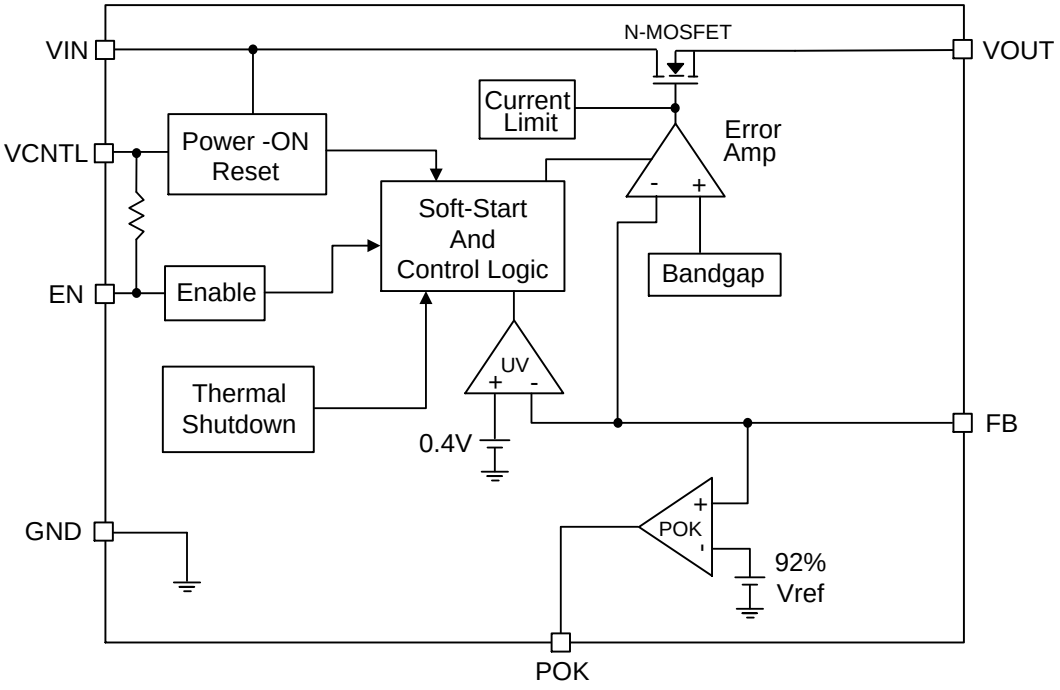
The AX6615 is a 3A ultra low dropout linear regulator. This product is specifically designed to provide well supply voltage for front-side-bus termination on motherboards and NB applications. The IC needs two supply voltages, a control voltage for the circuitry and a main supply voltage for power conversion, to reduce power dissipation and provide extremely low dropout. The AX6615 integrates many functions. A Power-On-Reset (POR) circuit monitors both supply voltages to prevent wrong operations. A thermal shutdown and current limit functions protect the device against thermal and current over-loads. The AX6615 can be enabled by other power system. Pulling and holding the EN pin below 0.3V shuts off the output.

The AX6615 is available in SOP-8L-EP and TDFN-10L packages which features small size as an Exposed Pad to reduce the junction-to-case resistance, being applicable in 2~3W applications.

❖ FEATURES

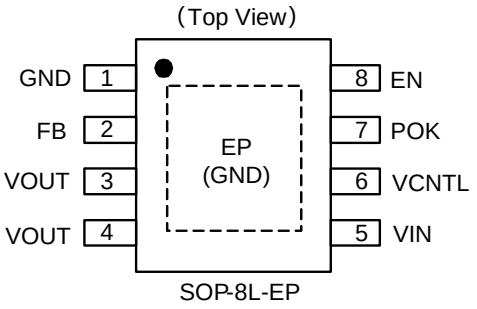
- Ultra Low Dropout - 0.23V(typical) at 3A Output Current
- Low ESR Output Capacitor (Multi-layer Chip Capacitors (MLCC)) Applicable
- 0.8V Reference Voltage
- Fast Transient Response
- Adjustable Output Voltage by External Resistors
- Power-On-Reset Monitoring on Both VCNTL and VIN Pins
- Internal Soft-Start
- Under-Voltage Protection
- Current-Limit and Thermal Shutdown Protection
- SOP-8L-EP and TDFN-10L (3mm*3mm) Pb-Free Package.
- RoHS and Halogen free compliance.

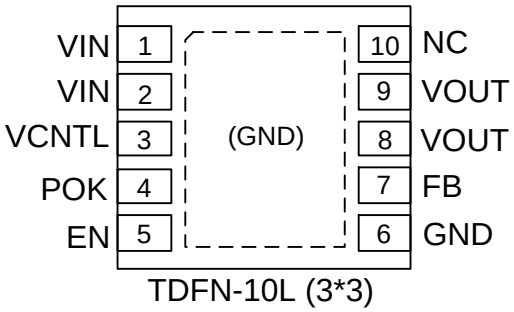
❖ BLOCK DIAGRAM



❖ PIN ASSIGNMENT

The packages of AX6615 are SOP-8L-EP and TDFN-10L; the pin assignment is given by:





Name	Description
GND	GND pin
FB	Feedback pin
V_{OUT}	IC power supply pin
EN	Internal Pull High. EN=high or Floating → Enable EN=Low → Shutdown mode
POK	Power OK Output Pin
VCNTL	CNTL Pin Input Voltage
VIN	Input Voltage
EP	Connect to to GND

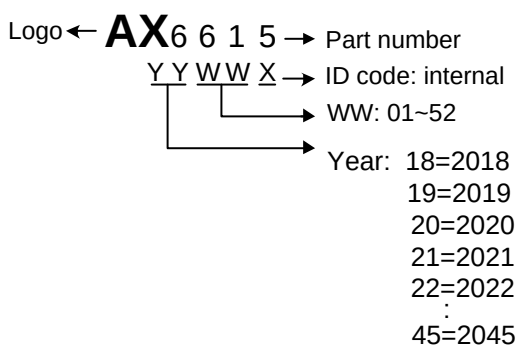
❖ ORDER/MARKING INFORMATION

Order Information

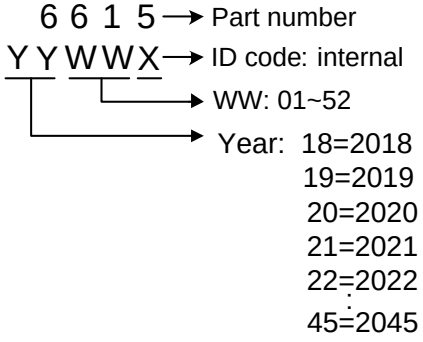
AX6615 XXX X

- XXX: Package Type — ES: SOP-8L-EP; J10: TDFN-10L(3*3)
- X: Packing — Blank: Tube; A: Taping

Top Marking (SOP-8L-EP)



Top Marking (TDFN-10L)



❖ ABSOLUTE MAXIMUM RATINGS (at T_A=25°C)

Characteristics		Symbol	Rating	Unit
V_{CNTL} Supply Voltage		V_{CNTL}	-0.3 to 7	V
V_{IN} Supply Voltage		V_{IN}	-0.3 to 6	V
EN and FB Pin Voltage		$V_{I/O}$	-0.3 to V_{CNTL}+0.3	V
Power good Voltage		V_{POK}	-0.3 to 7	V
Power Dissipation	SOP-8L-EP	PD	2.5	W
	TDFN-10L		2.2	
Storage Temperature Range		T_{ST}	-65 to +150	°C
Junction Temperature Range		T_J	-40 to 125	°C
Operating Temperature Range		T_{OP}	-40 to +85	°C
Thermal Resistance from Junction to case	SOP-8L-EP	θ_{JC}	15	°C/W
	TDFN-10L			
Thermal Resistance from Junction to ambient	SOP-8L-EP	θ_{JA}	40	°C/W
	TDFN-10L		45	

Note: θ_{JA} is measured with the PCB copper area (need connect to Expose-Pad) of approximately 1.5 in^2 (Multi-layer)

❖ RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Conditions	Rating	Unit
V_{CNTL} Supply Voltage	V_{CNTL}		3 to 5.5	V
V_{IN} Supply Voltage	V_{IN}		1.2 to 3.65	V
Output Voltage	V_{OUT}	V_{CNTL}-V_{OUT}>1.9V	0.8 to V_{IN}-V_{DROP}	V
Output Current	I_{OUT}		0 to 3	A

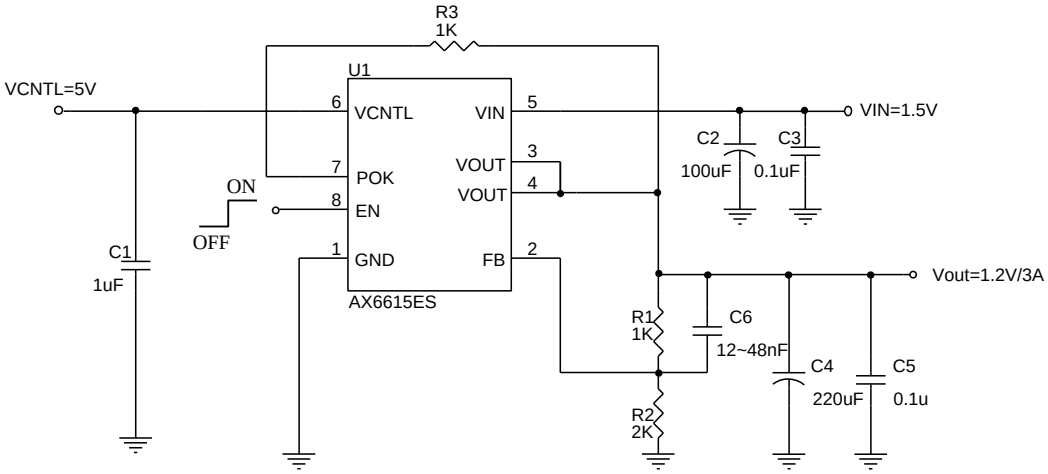
❖ ELECTRICAL CHARACTERISTICS

(V_{CNTL} = 5V, V_{IN} = 1.5V, V_{OUT} = 1.2V, T_A=25°C unless otherwise specified)

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
V_{CNTL} POR Threshold	V_{CNTL}		2.5	2.7	2.9	V
V_{CNTL} POR Hysteresis	$V_{CNTL(hys)}$		-	0.4	-	V
V_{IN} POR Threshold	V_{IN}		0.8	0.9	1.0	V
V_{IN} POR Hysteresis	$V_{IN(hys)}$		-	0.5	-	V
V_{CNTL} Nominal Supply Current	I_{CNTL}	EN= V_{CNTL}	-	1	1.8	mA
V_{CNTL} Shuntdown Current	I_{SD}	EN= 0V	-	15	30	uA
Feedback Voltage	V_{FB}	V_{CNTL}=5V, I_{OUT} =10mA	0.788	0.8	0.812	V
Load Regulation		I_{OUT}=0A ~ 3A	-	0.06	0.25	%
Line Regulation		V_{CNTL}= V_{EN} =5V V_{IN} = V_{OUT} + 0.5V~5V I_{OUT} =10mA	-	0.01	0.1	%/V
Dropout Voltage	V_{DROP}	I_{OUT} = 3A, V_{CNTL}=5V; V_{OUT}=1.2V	-	0.23	0.28	V
V_{OUT} Pull Low Resistance		EN=0V	-	85	-	Ω
Soft Start Time	T_{SS}		-	2	4	mS
EN Pin Logic High threshold voltage	V_{ENH}	Enable	1.2	-	-	V
	V_{ENL}	Disable	-	-	0.4	
EN Hysteresis			-	50	-	mV
EN Pin Pull-Up Current	I_{EN}	EN=GND	-	10	-	uA
Current Limit	I_{LIM}	V_{CNTL}=3~5.5V T_J= -40 ~ 125°C	3.3	-	-	A
Ripple Rejection V_{IN}	PSRR	F=120Hz, I_{OUT}=100mA	-	65	-	dB
Ripple Rejection V_{CNTL}			-	65	-	
Under-Voltage Threshold		VFB Falling	-	0.4	-	V
POK Threshold Voltage for Power OK	V_{POK}	VFB Rising	89%	92%	95%	VFB
POK Threshold Voltage for Power Not OK	V_{PNOK}	VFB Falling	78%	81%	84%	VFB
POK Low Voltage		POK sinks 5mA	-	0.25	0.4	V
Thermal shutdown Temp	T_{SD}		-	160	-	°C
Thermal Shutdown Hysteresis	T_{SH}		-	50	-	°C

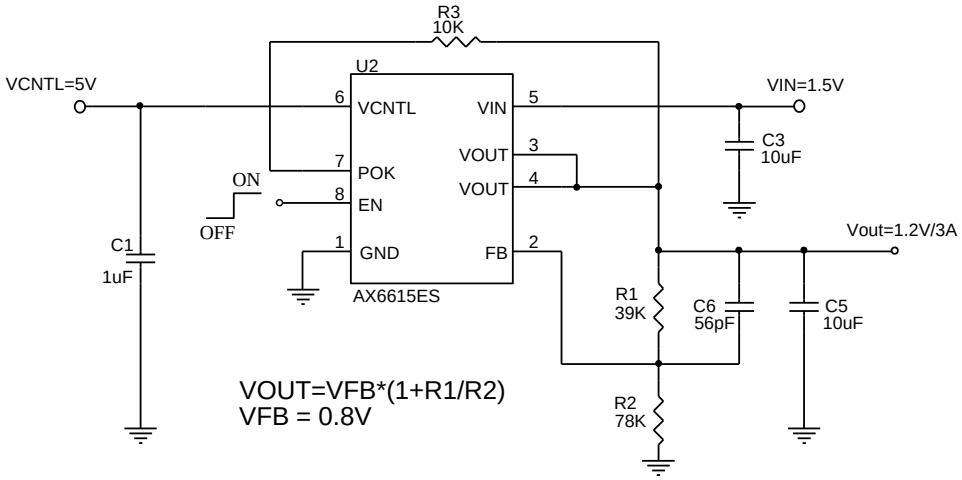
❖ APPLICATION CIRCUIT

1. Using an Output Capacitor with ESR≧20mΩ

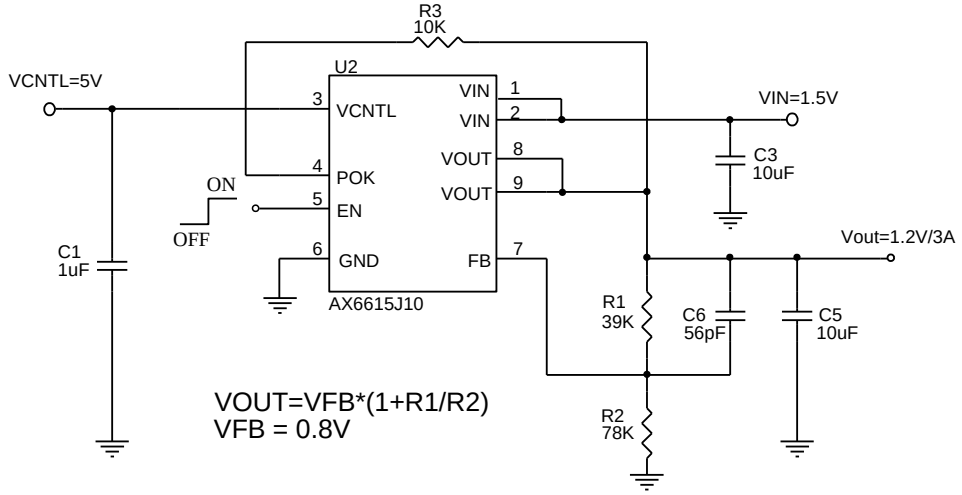


2. Using an MLCC as the Output Capacitor

SOP-8L-EP



TDFN-10L



❖ FUNCTION PIN DESCRIPTIONS

FB

Connecting this pin to an external resistor divider receives the feedback voltage of the regulator. The output voltage set by the resistor divider is determined by:

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2}\right) \quad (V)$$

Where R1 is connected from V_{OUT} to FB with Kelvin sensing and R2 is connected from FB to GND. A bypass capacitor may be connected with R1in parallel to improve load transient response. The recommended R2 and R1 are in the range of 1K~100KΩ.

VIN

Main supply input pins for power conversions. The voltage at this pin is monitored for Power-On Reset purpose.

VCNTL

Power input pin of the control circuitry. Connecting this pin to a +5V (recommended) supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On Reset purpose.

POK

Power-OK signal output pin. This pin is an open-drain output used to indicate status of output voltage by sensing FB voltage. This pin is pulled low when the rising FB voltage is not above the V_{POK} threshold or the falling FB voltage is below the V_{POK} threshold, indicating the output is not OK.

EN

Enable control pin. Pulling and holding this pin below 0.3V shuts down the output. When re-enabled, the IC undergoes a new soft-start cycle. Left this pin open, this pin is internal pulled up to V_{CNTL} voltage, enabling the regulator.

VOUT

Output of the regulator. Please connect Pin 3 and Pin 4 using wide tracks. It is necessary to connect an output capacitor with this pin for closed-loop compensation and improving transient responses.

❖ FUNCTION DESCRIPTIONS

Power-On-Reset

A Power-On-Reset (POR) circuit monitors both input voltages at $V_{CNT}L$ and V_{IN} pins to prevent wrong logic controls. The POR function initiates a soft-start process after the two supply voltages exceed their rising POR threshold voltages during powering on. The POR function also pulls low the POK pin regardless the output voltage when the V_{CNTL} voltage falls below its falling POR threshold.

Internal Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 2mS.

Output Voltage Regulation

An error amplifier working with a temperature compensated 0.8V reference and an output NMOS regulates output to the preset voltage. The error amplifier designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from V_{IN} to V_{OUT}.

Current-Limit

The AX6615 monitors the current via the output NMOS and limits the maximum current to prevent load and AX6615 from damages during overload or short circuit conditions.

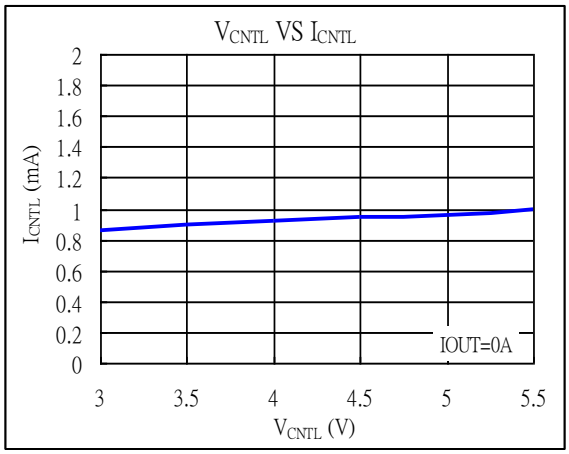
Under-Voltage Protection (UVP)

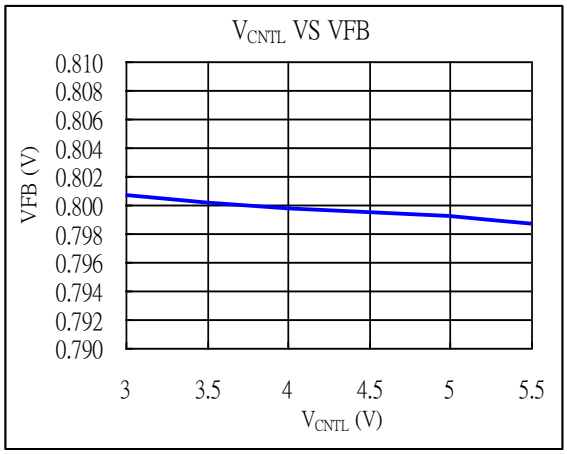
The AX6615 monitors the voltage on FB pin after soft-start process is finished. Therefore the UVP is disabling during soft-start. When the voltage on FB pin falls below the under-voltage threshold, the UVP circuit shuts off the output immediately. After a while, the AX6615 starts a new soft-start to regulate output.

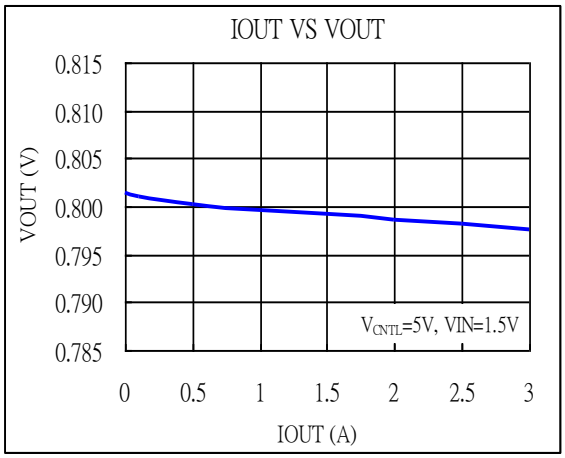
Thermal Shutdown

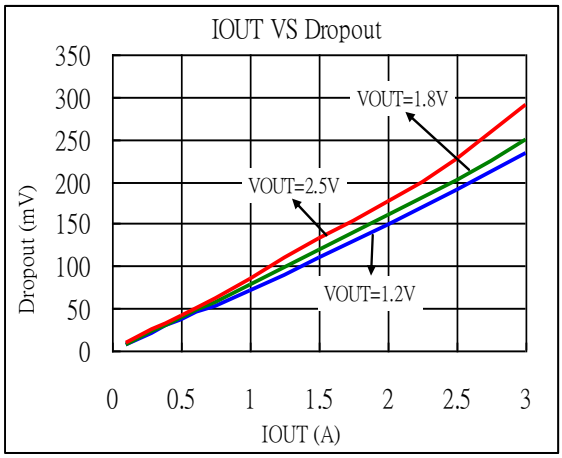
A thermal shutdown circuit limits the junction temperature of AX6615. When the junction temperature exceeds +150°C, a thermal sensor turns off the output NMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 50°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown designed.

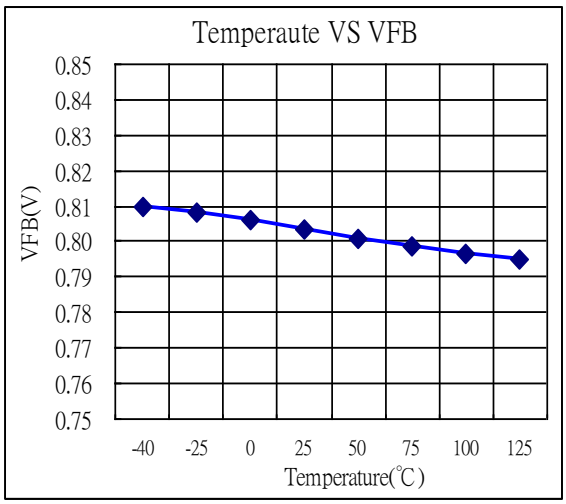
❖ TYPICAL CHARACTERISTICS

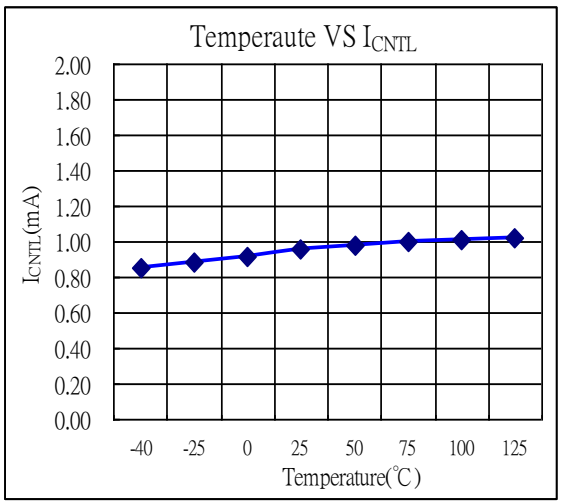






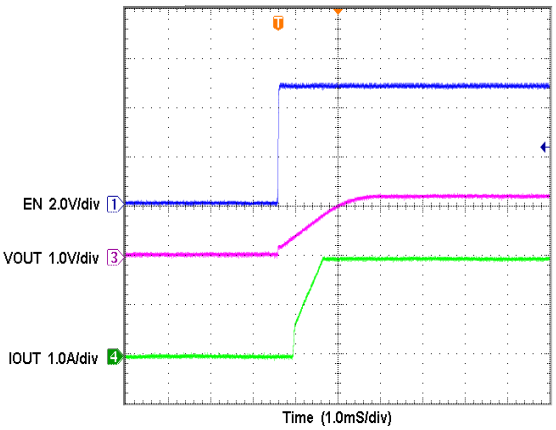




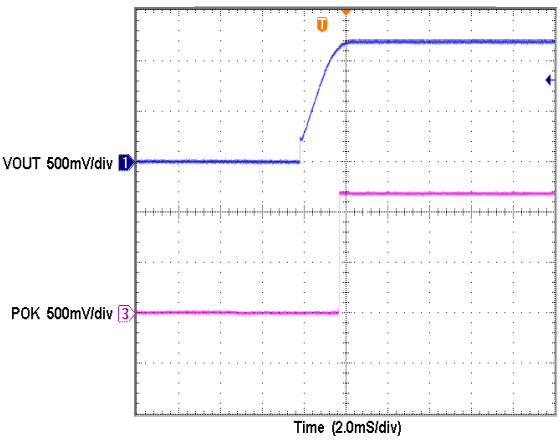


❖ TYPICAL CHARACTERISTICS (CONTINUES)

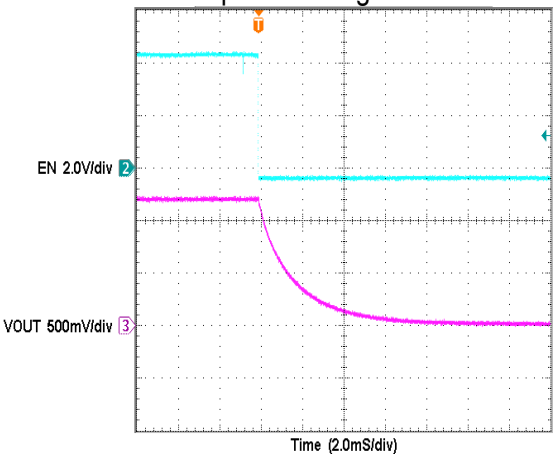
Enable-ON



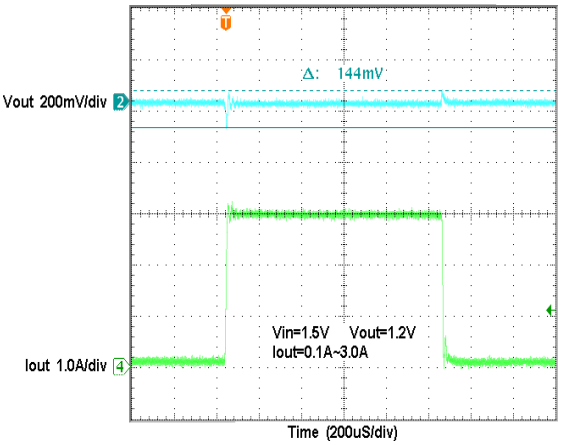
Power OK Wave



Output Discharge

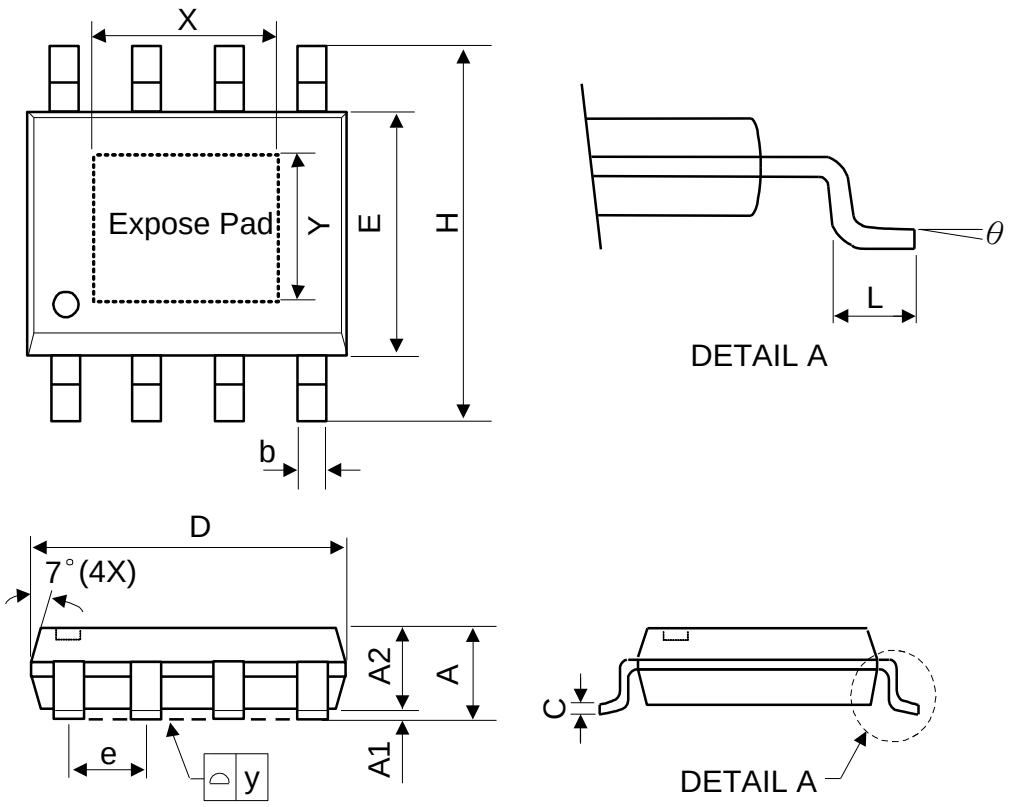


Load Transient



❖ PACKAGE OUTLINES

(1) SOP-8L-EP

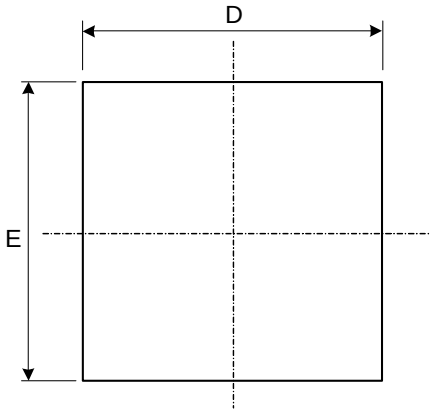


Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.75	-	-	0.069
A1	0	-	0.15	0	-	0.06
A2	1.25	-	-	0.049	-	-
C	0.1	0.2	0.25	0.0075	0.008	0.01
D	4.7	4.9	5.1	0.185	0.193	0.2
E	3.7	3.9	4.1	0.146	0.154	0.161
H	5.8	6	6.2	0.228	0.236	0.244
L	0.4	-	1.27	0.015	-	0.05
b	0.31	0.41	0.51	0.012	0.016	0.02
e	1.27 BSC			0.050 BSC		
y	-	-	0.1	-	-	0.004
X	-	2.34	-	-	0.092	-
Y	-	2.34	-	-	0.092	-
θ	0°	-	8°	0°	-	8°

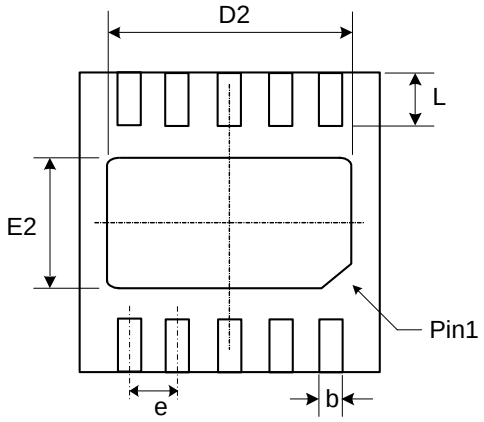
Mold flash shall not exceed 0.25mm per side

JEDEC outline: MS-012 BA

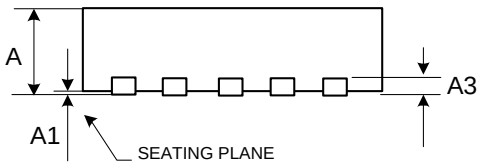
(2) TDFN-10L (3*3 0.75mm)



(Top View)



(Bottom View)

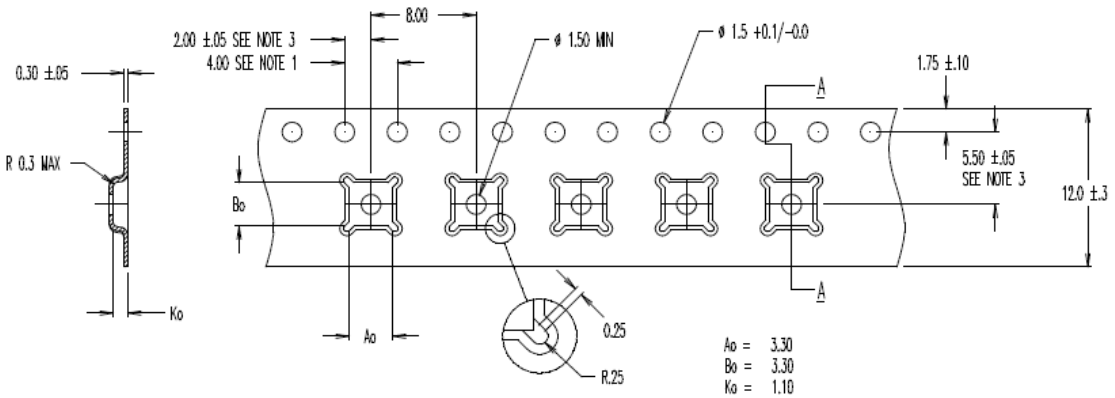


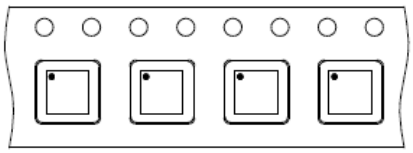
(SIDE View)

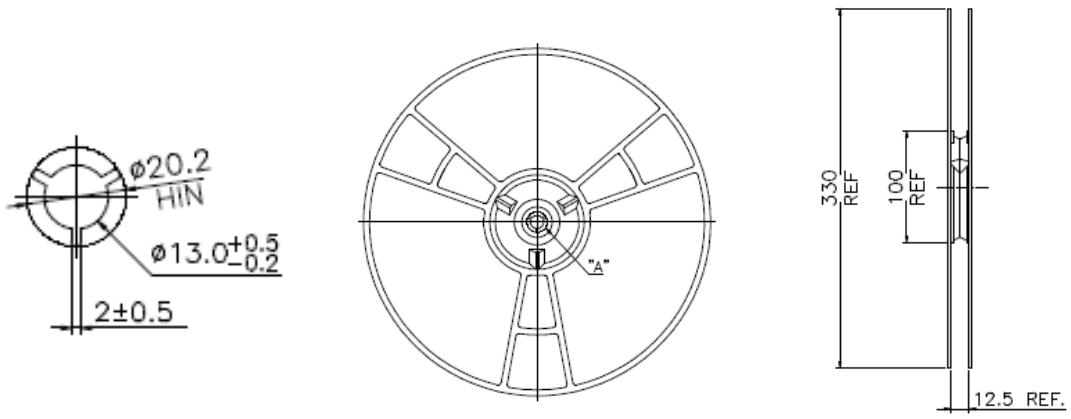
Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF.			0.008 REF.		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.20	2.40	2.50	0.087	0.094	0.098
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.50	1.60	1.70	0.059	0.063	0.070
e	0.50 BSC.			0.020 BSC.		
L	0.30	0.40	0.50	0.012	0.016	0.020

❖ Carrier tape dimension

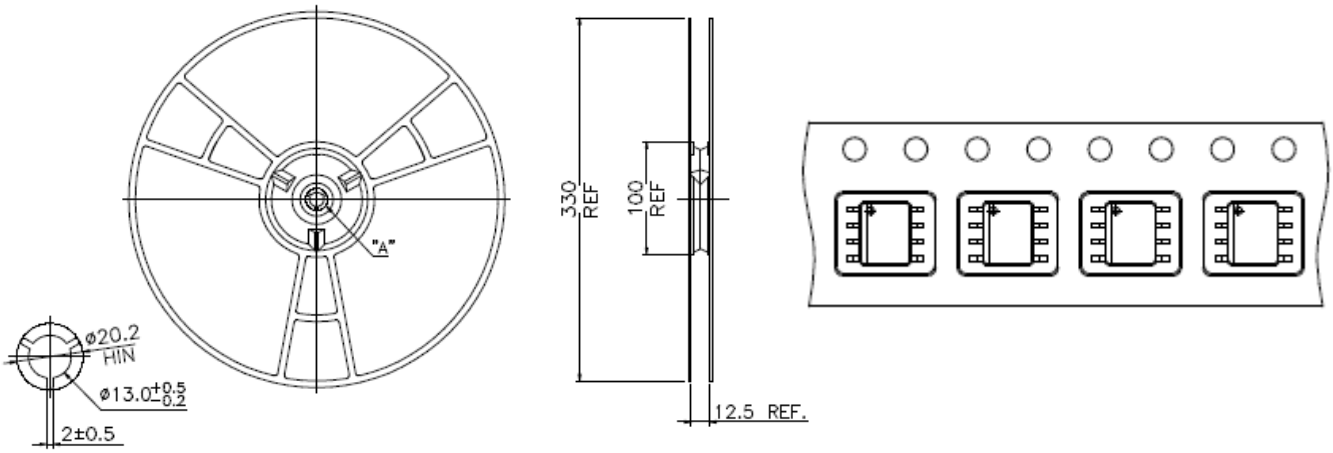
TDFN-10L(3x3mm)

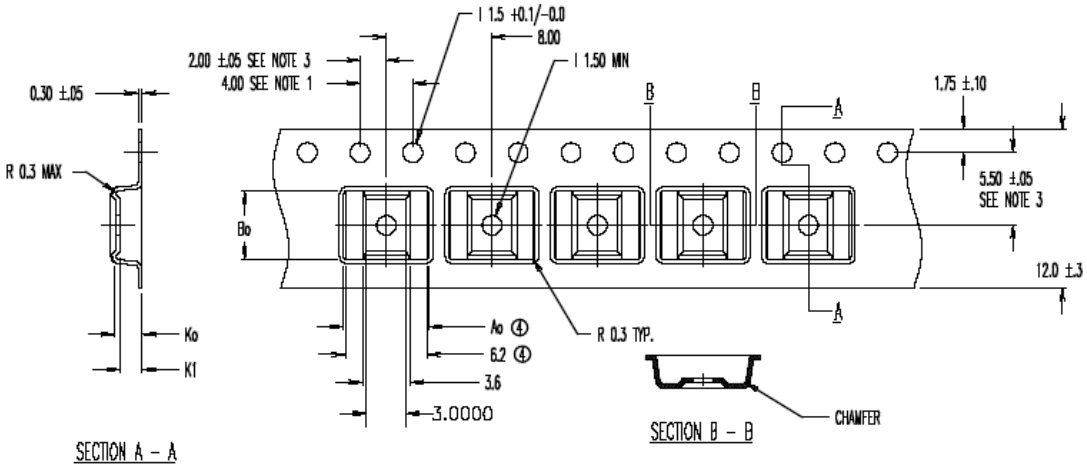






SOP-8L-EP





④① Ao = 6.50
Bo = 5.20
Ko = 2.10
K1 = 1.70

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2mm
2. Camber not to exceed 1mm in 100mm.
3. Material: Anti–Static Black Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.