-30V Dual P-Channel Enhancement Mode MOSFET

❖ DESCRIPTION

The AM4953 is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

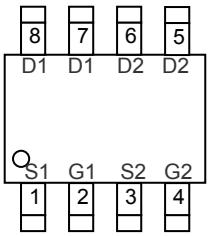
❖ APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

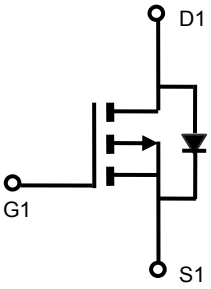
❖ FEATURE

- ***-30V/-5.2A, $R_{DS(ON)}$ < 60mΩ@V_{GS} = -10V***
- ***-30V/-4.5A, $R_{DS(ON)}$ <90mΩ@V_{GS} = -4.5V***
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Full RoHS compliance
- SOP-8 package design

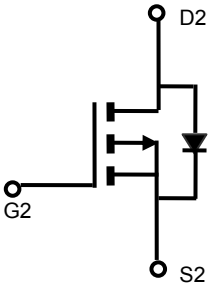
❖ PIN CONFIGURATION



TOP VIEW
SOP-8



P-Channel



P-Channel

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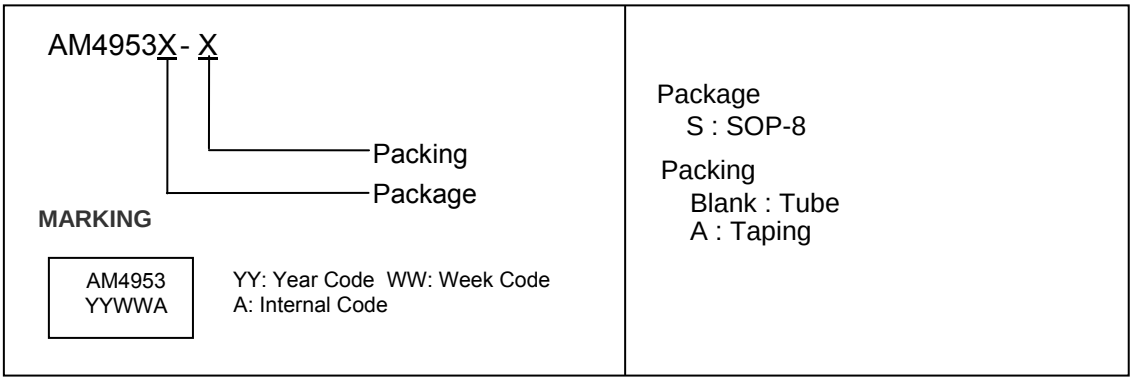
❖ PART MARKING INFORMATION



❖ PART MARKING INFORMATION

Part Number	Package Code	Package	Shipping
AM4953S-A	S	SOP-8	2500 /Tape&Reel

※ Year Code : 00 ~ 99
※ Week Code : 01~52
※ SOP-8 : Only available in tape and reel packaging. (A reel contains 2500 devices)
※ G : Lead-free product. This product is RoHS compliant

❖ ABSOLUTE MAXIMUM RATINGS (T_A = 25℃ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current (T_J=150℃)	V_{GS} = -10V	-5.2	A
I_{DM}	Pulsed Drain Current		-20	A
I_S	Continuous Source Current (Diode Conduction)		-2.4	A
T_J	Operation Junction Temperature		-55~150	℃
T_{STG}	Storage Temperature Range		-55~150	℃
P_D	Power Dissipation	T_A=25℃ T_A=70℃	2.8 1.8	W
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		70	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

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❖ ELECTRICAL CHARACTERISTICS(T_A = 25℃ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS} =0V,I_D =-250μA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} =V_{GS},I_D =-250μA	-1.0		-3.0	V
I_{GSS}	Gate Leakage Current	V_{DS} =0V,V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =-30V,V_{GS} =0V			-1	μA
		V_{DS} =-30V,V_{GS} =0V T_J =55℃			-5	
$I_{D(ON)}$	On-State Drain Current	V_{DS} ≦-5V,V_{GS} ≦-10V	-25			A
$R_{DS(ON)}$	Drain-source On-Resistance	V_{GS} =-10V,I_D=-5.2A V_{GS} =-4.5V, I_D=-4.5A		45 60	60 90	mΩ
G_{fs}	Forward Transconductance	V_{DS} =-10V,I_D =-5.2A		10		S
Source-Drain Doide						
Is	Diode forward Current (Max.)				2.6	A
V_{SD}	Diode Forward Voltage	I_S=-2.0A,V_{GS}=0V		-0.8	-1.2	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS} =-15V,V_{GS} =-10V I_D =-5.0A		15	10	nC
Q_{gs}	Gate-Source Charge			4.0		
Q_{gd}	Gate-Drain Charge			2.0		
C_{iss}	Input Capacitance	V_{DS} =-15V,V_{GS} =0V f =1MHz		680		pF
C_{oss}	Output Capacitance			120		
C_{rss}	Reverse Transfer Capacitance			75		
$t_{d(on)}$	Turn-On Time	V_{DD} =-15V,R_L =15Ω I_D =-1.0A,V_{GEN} =-10V R_G =6Ω		7.0	15	nS
t_r				10	20	
$t_{d(off)}$	Turn-Off Time			40	80	
t_f				20	40	

Note : 1. Pulse test: pulse width <= 300us, duty cycle<= 2%
2. Static parameters are based on package level with recommended wire-bonding

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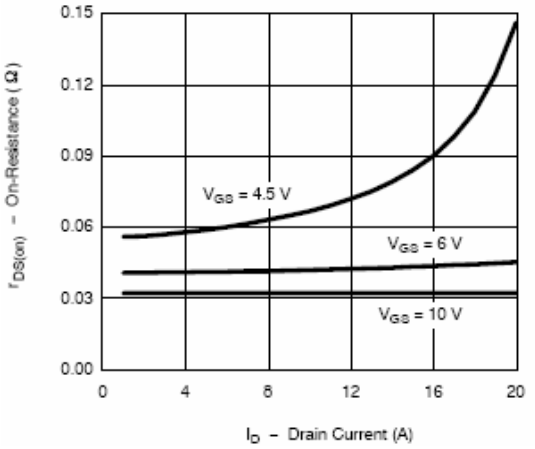
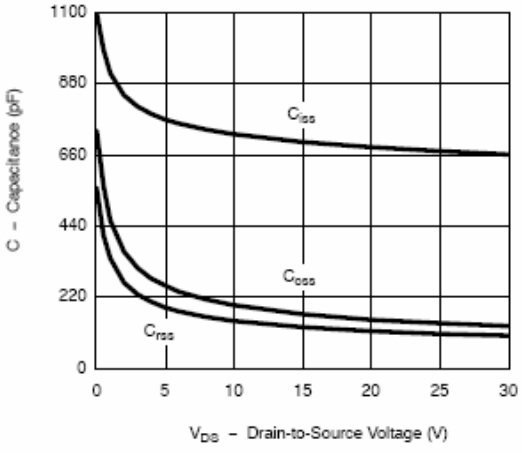
❖ TYPICAL CHARACTERISTICS (25℃ Unless Note)

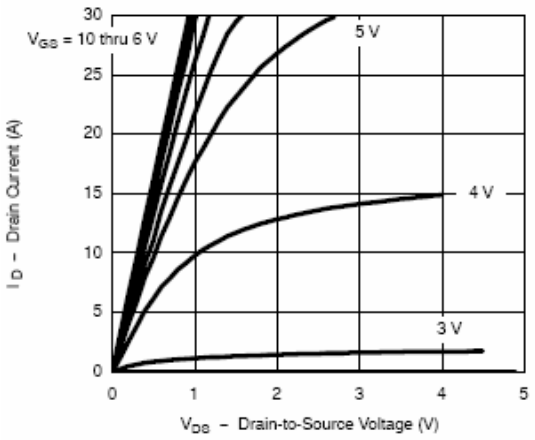
On-Resistance vs. Drain Current



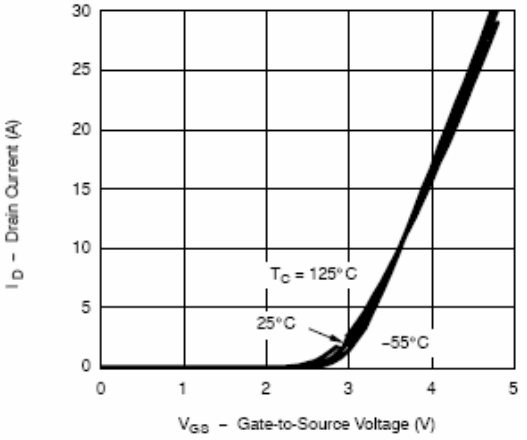
Capacitance



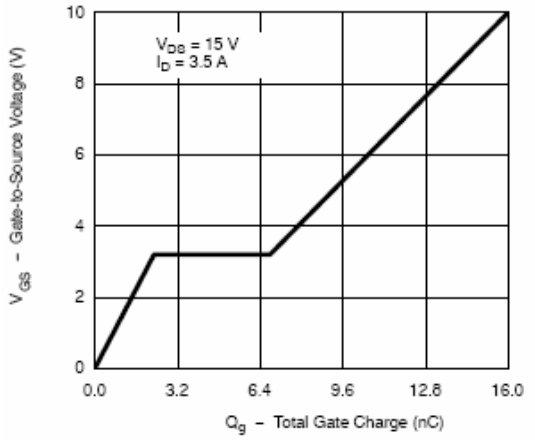
Output Characteristics



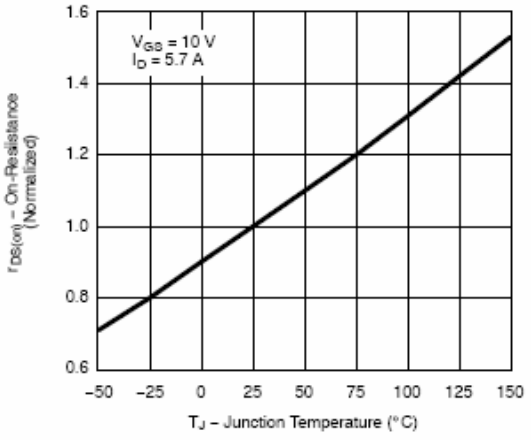
Transfer Characteristics



Gate Charge



On-Resistance vs. Junction Temperature



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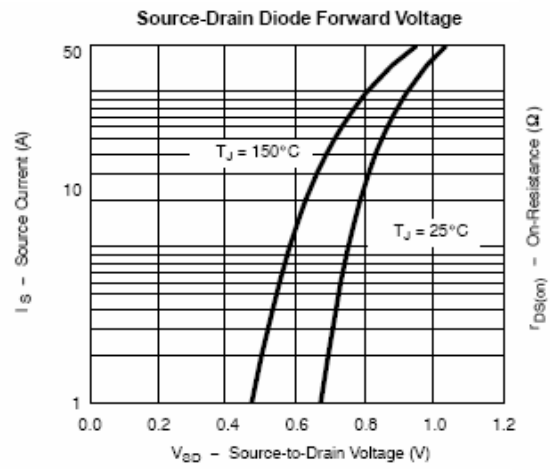

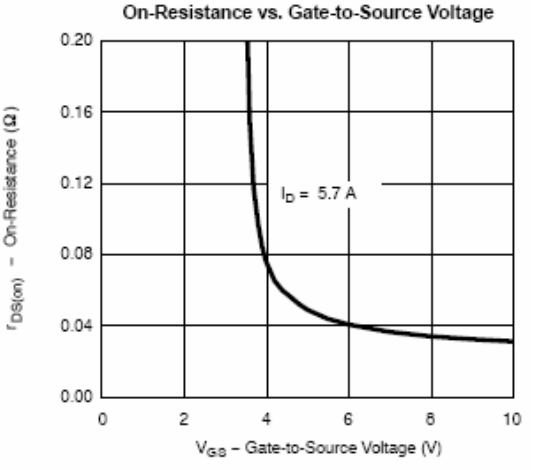

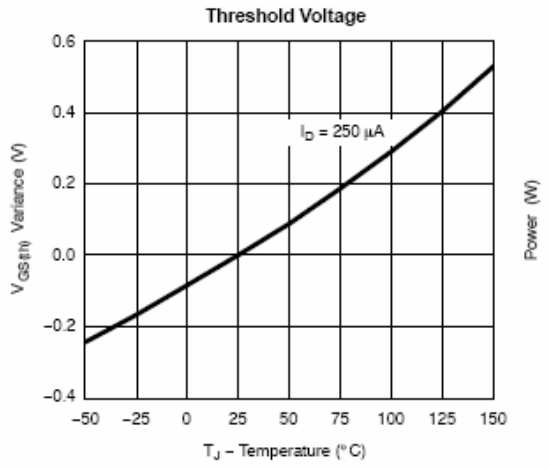

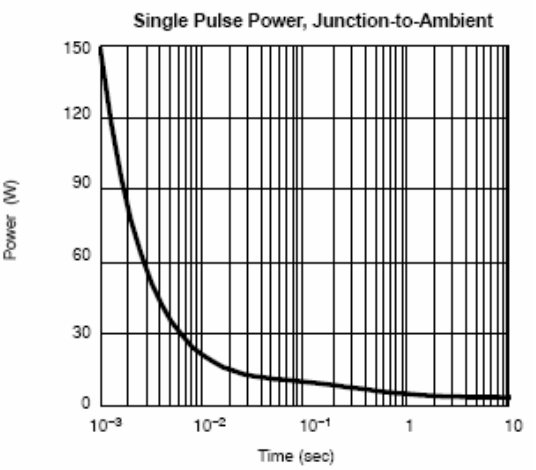

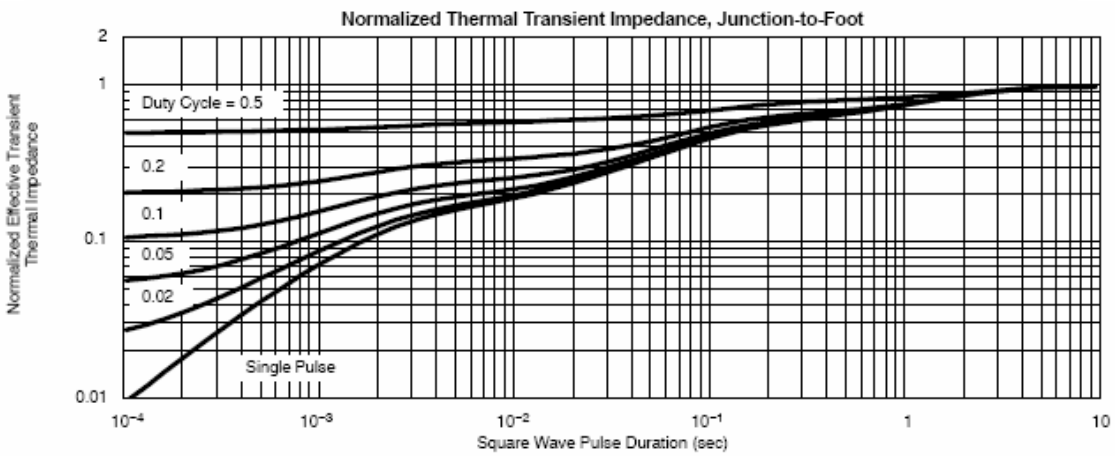

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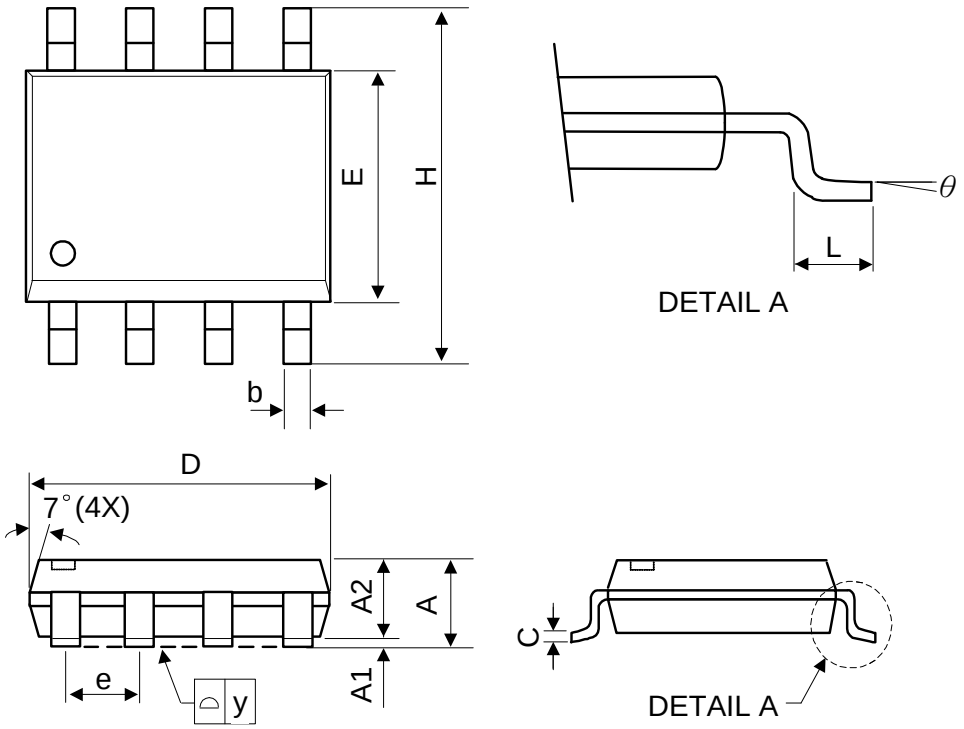
❖ PACKAGE OUTLINES



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.75	-	-	0.069
A1	0.1	-	0.25	0.04	-	0.1
A2	1.25	-	-	0.049	-	-
C	0.1	0.2	0.25	0.0075	0.008	0.01
D	4.7	4.9	5.1	0.185	0.193	0.2
E	3.7	3.9	4.1	0.146	0.154	0.161
H	5.8	6	6.2	0.228	0.236	0.244
L	0.4	-	1.27	0.015	-	0.05
b	0.31	0.41	0.51	0.012	0.016	0.02
e	1.27 BSC			0.050 BSC		
y	-	-	0.1	-	-	0.004
θ	0°	-	8°	0°	-	8°

Mold flash shall not exceed 0.25mm per side
JEDEC outline: MS-012 AA

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